VIAVI Solutions

VIAVI
ONT-600/800

KP4 FEC on N-PORT Module

Support for next generation, single lambda 100GE pluggables with KP4 FEC and 100GAUI-4

100G-DR (500 m on a single mode fiber) and 100G-FR/LR (up to 2/10 km on SMF) are part of the IEEE standard 802.3cd for 100GE serial transmission. A 100G-DR transponder carries the 100GE signal on a single lambda, using a rate of 53.125 GBaud with PAM-4 modulation and KP4 FEC - RS(544, 514). The solution described here also applies to 100G-FR/LR transponders (up to 2/10 km on SMF) that use 100GAUI-4 at the electrical side.

100G-DR signals are also used by 400G-DR4 transponders with 4 x 100G-DR breakout.

100G-DR transponders with the QSFP28 form factor can plug into standard, non-FEC (4 x 25.78 Gbit/s NRZ) QSFP28 cages, since they have their FEC on-board.

Typically, these transponders also have FEC bypass capability that can be activated via the I2C control interface. In this mode, the FEC needs to be done on the host board itself.

The ONT N-PORT module supports this mode, such that the electrical input into the DR transponder is a 4 x 26.5625 Gbit/s signal with KP4 FEC. This means that the ONT has full control of all FEC Error insertion parameters, and allows to thoroughly test FEC based chips, transponders and systems that are connected to the (up to 4) 100G-DR transponders plugged into the VIAVI N-PORT module.
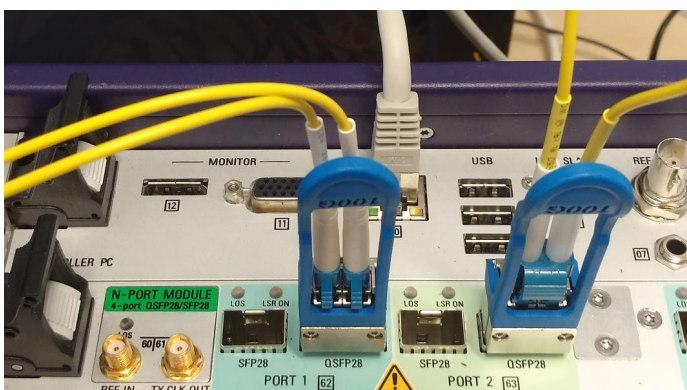
Benefits

- 4 x QSFP28 ports for independent 100GAUI-4 test
- RX FEC Error Statistics with Symbol Errors per Codeword allows link margin investigations and PAM-4 photonics characterization
- TX FEC Error Generation in Single, Rate and Burst modes
- Critical in-depth testing of IC FEC Logic and design with user defined FEC modes, FEC Stress, and FEC Power Integrity Stress Tests (needs "Ethernet FEC Validation", Option 401–820.60)

Applications

- 100G-DR IC and optical module validation and test
- 400G-DR4 breakout into 4 x 100G DR performance testing
- PAM-4 photonics performance investigations

100G

FEC

QSFP-DD

Test cases include:

- Assure correct functionality of the DUT's FEC algorithm when receiving correctable errors

- Check behavior of transponder when receiving uncorrectable FEC errors, but also in the presence of stress like clock offset or signal interrupts

- The KP4 FEC option allows to validate and stress DR links in a way not possible when just using a transponder module with inbuilt FEC

- A combination of the ONT support for the KP4 FEC and the ONT ability to inject random errors at the egress port allow the FEC performance of the FEC IC inside a module to be validated as well as deep diagnostic FEC information on the PAM-4 optical performance

Typical Test Setup

Schematic Block Diagram
VIAVI ONT-800

100G-DR Transponders
in FEC Bypass Mode
(FEC comes from ONT)
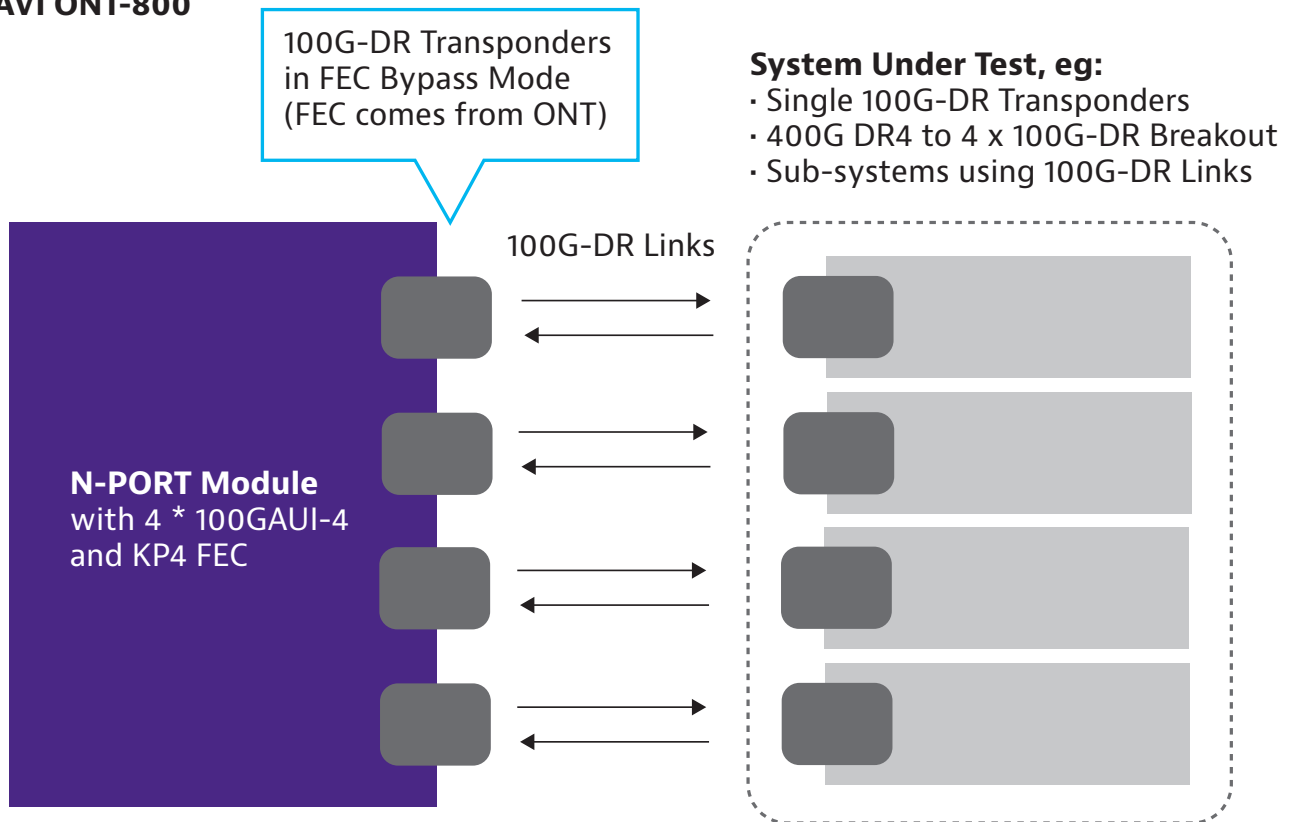
System Under Test, eg:
· Single 100G-DR Transponders
· 400G DR4 to 4 x 100G-DR Breakout
· Sub-systems using 100G-DR Links

100G-DR Links

N-PORT Module
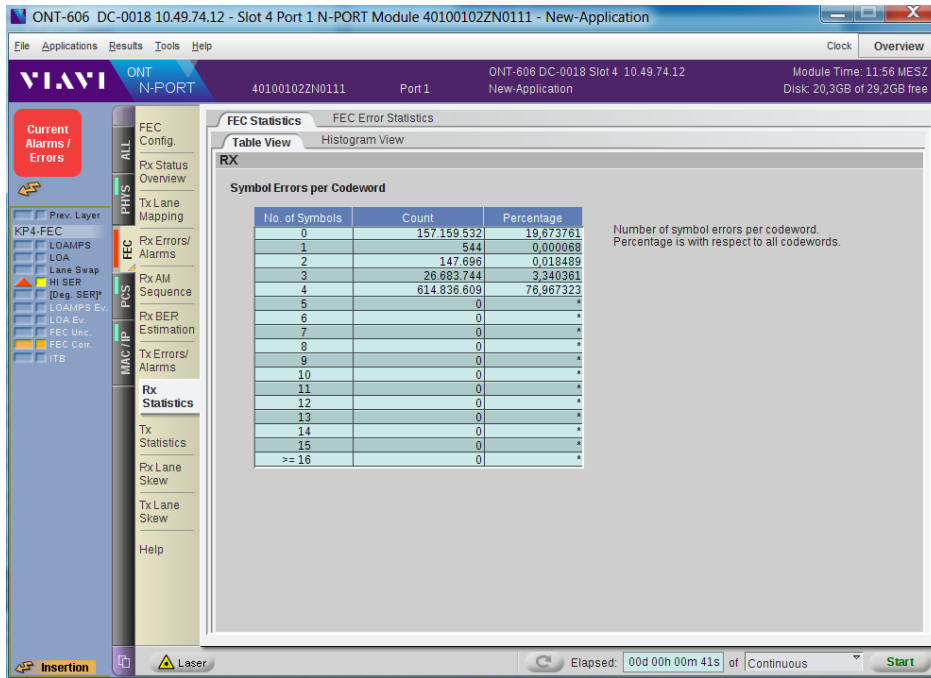with 4 * 100GAUI-4
and KP4 FEC

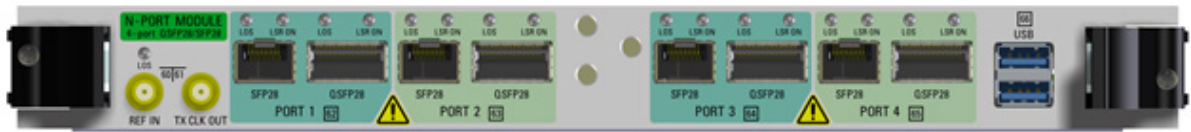Figure 1 - N-PORT RX FEC Statistics, running FEC Stress Test with up to 15 correctable Symbol Errors per Codeword

Figure 2 - N-PORT Module for ONT-800

Ordering Information

Modules

Part Number	Module Variant
401-001.01	N-PORT Module for ONT-800 platform 1 slot 4 ports
401-002.01	N-PORT Ethernet Module for ONT-800 platform 1 slots 4 ports
401-001.02	N-PORT Module for ONT-600 platform 2 slots 4 ports
401-002.02	N-PORT Ethernet Module for ONT-600 platform 2 slots 4 ports

Software Options

Part Number	SW Option
401-121.50	100GigE – 802.3cd – 100GAUI4 – NRZ – quad port
401-120.50	100GigE incl. Clause 91 FEC – quad port
401-820.60	Ethernet FEC Validation – Module Option